CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor device comprising a first chip and a second chip, said first and second chips being manufactured by mutually different manufacturing processes and packed in a single package, wherein said first chip includes:

a control circuit for generating control signals for operating said second chip; and

a test control circuit for inhibiting said control signals from being transmitted to said second chip while said first chip is tested.

2. The semiconductor device according to claim 1, comprising:

a first power supply terminal intended for said first chip; and

a second power supply terminal intended for said second chip, wherein

said test control circuit controls output of all of said control signals to be supplied to said second chip.

3. The semiconductor device according to claim 1, comprising

a power supply terminal common to said first chip and said second chip, wherein

said test control circuit controls output of an enable signal, said enable signal activating said second chip and being one of said control signals to be supplied to said second chip.

4. The semiconductor device according to claim 1, wherein said first chip includes:

a test terminal for receiving a test signal for putting said first chip into a test mode;

an input terminal for receiving an input signal which is used in a normal operation; and

a test starting circuit being activated upon reception of said test signal, and outputting a test starting signal in accordance with a logic of a signal input to said input terminal; and

said test control circuit inhibits transmission of said control signals when receiving said test starting signal.

5. The semiconductor device according to claim 1, wherein said first chip includes:

an input terminal for receiving an input signal which is used in a normal operation; and

a test starting circuit for outputting a test starting signal in accordance with a combination of logics of signals which are input to said input terminal a plurality of times; and

said test control circuit inhibits transmission of said control signals when receiving said test starting signal.

6. The semiconductor device according to claim 1, comprising

a test starting terminal for receiving a test starting signal for testing said first chip, wherein

said test control circuit inhibits transmission of said control signals when receiving said test starting signal.

7. The semiconductor device according to claim 1, wherein

said test control circuit includes output inhibition circuits for setting output nodes of said control signals to be in a high impedance state while said first chip is tested.

8. The semiconductor device according to claim 1, wherein

said test control circuit includes high level fixing circuits for fixing a level of output nodes of said control signals to high level while said first chip is tested.

9. The semiconductor device according to claim 1, wherein

said test control circuit includes low level fixing circuits for fixing a level of output nodes of said control signals to low level while said first chip is tested.

10. The semiconductor device according to claim 1, wherein:

said first chip is a logic chip; and

said second chip is a memory chip.

11. A semiconductor device comprising a first chip and a second chip, said first and second chips being manufactured by mutually different manufacturing processes and packed in a single package, comprising:

a first power supply terminal intended for an internal circuit of said first chip;

a second power supply terminal intended for an internal circuit of said second chip; and

a third power supply terminal intended for input/output circuits of said first and second chips, wherein:

said first chip includes a control circuit for generating control signals for operating said second chip;

said second chip includes a test control circuit being operative on a power supply voltage supplied to said third power supply terminal, for inhibiting said control signals from being transmitted to the internal circuit of said second chip while said first chip is tested.

12. The semiconductor device according to claim 11, comprising

a test starting terminal for receiving a test starting signal for testing said first chip, wherein

said test control circuit inhibits transmission of said control signals when receiving said test starting signal.

13. The semiconductor device according to claim 11, wherein

said test control circuit includes output inhibition circuits for setting output nodes of said control signals to be in a high impedance state while said first chip is tested.

14. The semiconductor device according to claim 11, wherein:

said first chip is a logic chip; and

said second chip is a memory chip.

15. A semiconductor integrated circuit comprising:

a control circuit for generating control signals for operating semiconductor chips which are manufactured by mutually different manufacturing processes and packed in a single package; and

a test control circuit being operative in a test mode, for inhibiting output of said control signals.

16. The semiconductor integrated circuit according to claim 15, comprising

a test starting terminal for receiving a test starting signal, wherein

said test control circuit inhibits output of said control signals when receiving said test starting signal.

17. The semiconductor device according to claim 15, wherein

said test control circuit includes output inhibition circuits for setting output nodes of said control signals to be in a high impedance state while said first chip is tested.

18. The semiconductor device according to claim 15, wherein

said test control circuit includes high level fixing circuits for fixing a level of output nodes of said control signals to high level while said first chip is tested.

19. The semiconductor device according to claim 15, wherein

said test control circuit includes low level fixing circuits for fixing a level of output nodes of said control signals to low level while said first chip is tested.